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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,925	07/07/2003	Takahiro Kawano	239801US2	6929

22850 7590 01/11/2008

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
01/11/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/612,925	KAWANO ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,45-47 and 52-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,45-47 and 52-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claims 1-2, 4-5, 45-47 and 52-69 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of a connecting plate connected to the main electrodes (the source electrode) and not electrically connected to the gate wiring, as recited in claims 1 and 56, are unclear as to how a transistor cannot have its source electrically connected to the gate.

The claimed limitation of a second insulating film, as recited in claim 4, is unclear as to whether said second insulating film is the same second insulating film recited in claim 54 or a different element.

The claimed limitation of "the second insulating film", as recited in claim 46, is unclear as to structural relationship between the second insulating film and the semiconductor device.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-2, 4-5, 45-47 and 52-69 are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. Claims 1 and 56 recite a connecting plate connected to the main electrodes (the source electrode) and not electrically connected to the gate wiring. That is, the source electrode is not electrically connected to the gate wiring. One device, which comprises a transistor whose source and gate are not electrically connected is not operative since current cannot flow through the transistor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-5, 45-47 and 52-69, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara et al. (6,342,709) in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 1, Sugawara et al. teach in figure 1 and related text a semiconductor device comprising:

a semiconductor layer which includes a first semiconductor region 2 of a first conductivity type, a base region 4 of a second conductivity type formed above the first semiconductor region and a plurality of second semiconductor regions 5 of the first conductivity type formed on the first semiconductor base region;

a gate electrode 14 which is formed between the first semiconductor region and the second semiconductor regions and which is adjacent to the first semiconductor region and the second semiconductor regions, the gate electrode facing the base region via a gate insulating film 9;

a gate wiring Tg which is formed on the semiconductor layer via a first insulating film and which is made of metal, the gate wiring being electrically connected to the gate electrode;

a plurality of main electrodes 11, Ts which are electrically connected to the plurality of second semiconductor regions, wherein the gate wiring is arranged between the main electrodes and the gate wiring is not electrically connected to the main electrodes; and

the highest portion of an uppermost surface of the gate wiring Tg is not higher than the upper surfaces of the main electrode Ts.

Nagata et al. do not teach a connecting plate which is connected onto upper surfaces of the main electrodes, wherein the main electrodes are in contact with a contact region of

the connecting plate, wherein the connecting plate is connected to a lead frame and the gate wiring is not electrically connected to the connecting plate.

AAPA teaches in figure 21 and related text (page 3, lines 9-10) a connecting plate 2109 which is connected onto upper surfaces of the main electrodes, wherein the main electrodes are in contact with a contact region of the connecting plate, wherein the connecting plate is connected to a lead frame 2003 (see figure 20) and the gate wiring is not electrically connected to the connecting plate.

AAPA also teaches that the connecting plate replaces the wiring connecting the main electrodes of the device and the lead frame.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a connecting plate which is connected onto upper surfaces of the main electrodes, wherein the main electrodes are in contact with a contact region of the connecting plate, wherein the connecting plate is connected to a lead frame and the gate wiring is not electrically connected to the connecting plate in Sugawara et al.'s device, in order to operate the device in its intended use (by providing lead frame and external connections) and to reduce the contact resistance of the device by using a connecting plate between the electrodes and the lead frame, respectively.

The combination is motivated by the teachings of AAPA which points out the advantages of using a connecting plate instead of external wiring.

Note that in prior art's device, the highest portion of an uppermost surface of the gate wiring is not higher than the upper surfaces of the main electrodes is in an area under the contact region of the connecting plate.

Regarding claim 56, Sugawara et al. teach in figure 1 and related text a semiconductor device comprising:

a first semiconductor region 2 of a first conductive type;

a second semiconductor region 4 of a second conductive type, the second semiconductor region being formed above the first semiconductor region;

a third semiconductor region 5 of the first conductive type, the third semiconductor region being formed above the second semiconductor region;

a gate electrode 14 which is formed between the first semiconductor region and the third semiconductor region and which is adjacent to the first semiconductor region and the third semiconductor region, the gate electrode facing the second semiconductor region via a gate insulating film 9;

a first main electrode 11 which is divided into a plurality of first main electrode units, the first main electrode units being electrically connected to the second semiconductor region and the third semiconductor region;

a metal gate wiring Tg which is electrically connected to the gate electrode and which is arranged between the first main electrode units;

Nagata et al. do not teach a lead frame and a connecting plate which is connected to the first main electrode units and the lead frame by ultrasonic bonding so as to electrically connect the first main electrode units to the lead frame, the connecting plate being in the form of a plate, wherein the first main electrode units are connected to the connecting plate by the ultrasonic bonding such that the connecting plate covers at least a portion of the first main electrode units between which the metal gate wiring is

arranged, and wherein the metal gate wiring does not electrically connect to the connecting plate which is over the metal gate wiring.

AAPA teaches in figure 21 and related text (page 3, lines 9-10) a lead frame 2003 (see figure 20), and a connecting plate 2109 which is connected to the first main electrode units and the lead frame by ultrasonic bonding so as to electrically connect the first main electrode units to the lead frame, the connecting plate being in the form of a plate, wherein the first main electrode units are connected to the connecting plate by the ultrasonic bonding such that the connecting plate covers at least a portion of the first main electrode units between which the metal gate wiring is arranged, and wherein the metal gate wiring does not electrically connect to the connecting plate which is over the metal gate wiring.

AAPA also teaches that the connecting plate replaces the wiring connecting the main electrodes of the device and the lead frame.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a lead frame and a connecting plate which is connected to the first main electrode units and the lead frame so as to electrically connect the first main electrode units to the lead frame, the connecting plate being in the form of a plate, wherein the first main electrode units are connected to the connecting plate such that the connecting plate covers at least a portion of the first main electrode units between which the metal gate wiring is arranged, and wherein the metal gate wiring does not electrically connect to the connecting plate which is over the metal gate wiring in Sugawara et al.'s device, in order to operate the device in its intended use (by providing

lead frame and external connections) and to reduce the contact resistance of the device by using a connecting plate between the electrodes and the lead frame, respectively. The combination is motivated by the teachings of AAPA which points out the advantages of using a connecting plate instead of external wiring.

Regarding the process limitations ("the first connecting plate is connected to the first main electrode and the second main electrode by ultrasonic bonding" and "the first main electrode units are connected to the connecting plate by the ultrasonic bonding") these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 2 and 5, Sugawara et al. teach the uppermost surfaces of the plurality of the main electrodes are a metal, wherein the plurality of main electrodes are formed apart from the gate wiring with a gap there between.

Regarding claims 4, 46, 54 and 59, prior art's device comprises a second insulating film (see AAPA) is formed on the gate wiring so as to insulate the gate wiring from the connecting plate, and the second main electrode is formed on the second insulating film.

Regarding claims 45, 47 and 55, the claimed limitations of main electrodes comprise a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, wherein the second main electrode is thicker than the first main electrode layer, these features are inherent in prior art's device, because the first main electrode layer is not necessarily distinguishable from the second main electrode layer. Thus, the main electrodes of prior art's device can be arbitrarily divided into a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, wherein the second main electrode is thicker than the first main electrode layer, as claimed.

Regarding claims 52-53, 55 and 57-58, prior art's device comprises the upper surfaces of the main electrodes are higher than the highest portion of an uppermost surface of the gate wiring, wherein the connecting plate is directly connected onto the upper

surfaces of the main electrodes (AAPA further teaches in figure 20 and related text a wiring 2004 is directly connected between the main electrodes of the device 2002 and the lead frame 2003), wherein the highest portion of an uppermost surface of the metal gate wiring is lower than a bottom surface of a portion of the connecting plate which is over the metal gate wiring.

Regarding claims 60-62, prior art's device comprises a fourth semiconductor region of the second conductive type, the fourth semiconductor region being formed on a side of the first semiconductor region which is opposite to the second semiconductor region, and a second main electrode which is formed on a side of the first semiconductor region which is opposite to the second semiconductor region, the second main electrode being electrically connected to the first semiconductor region.

Regarding claims 63-64, 66 and 68-69, Sugawara et al. teach the gate electrode is formed in a trench with the gate insulating film, wherein the trench passes through the second semiconductor region so as to reach the first semiconductor region, wherein

the connecting plate is made of aluminum, wherein

a gap is formed between the first main electrode units and the metal gate wiring, and wherein

the semiconductor device is a vertical MOSFET and an IGBT.

Regarding claims 65 and 67, prior art's device comprises a connecting plate covers a major part of the first main electrode units, wherein the connecting plate is directly connected to the first main electrode units and the lead frame.

Response to Arguments

Applicant's arguments with respect to claims 1-2, 4-5, 45-47 and 52-69 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
1/7/08

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